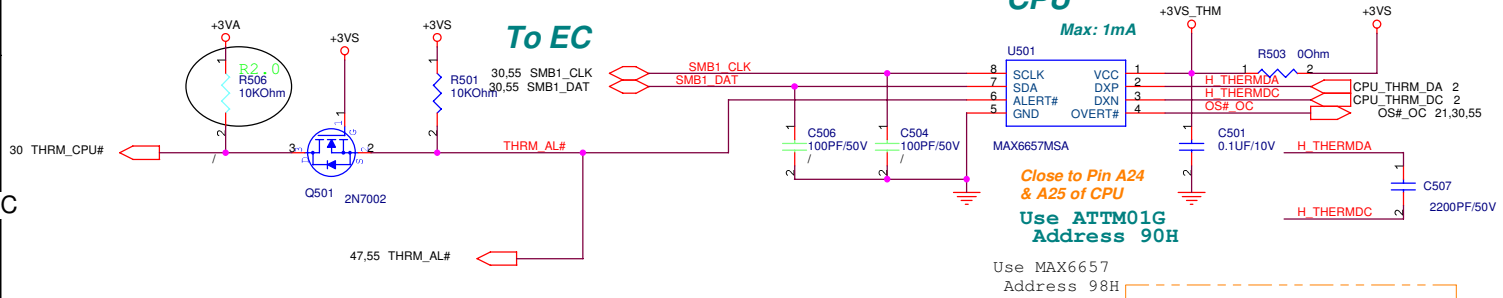


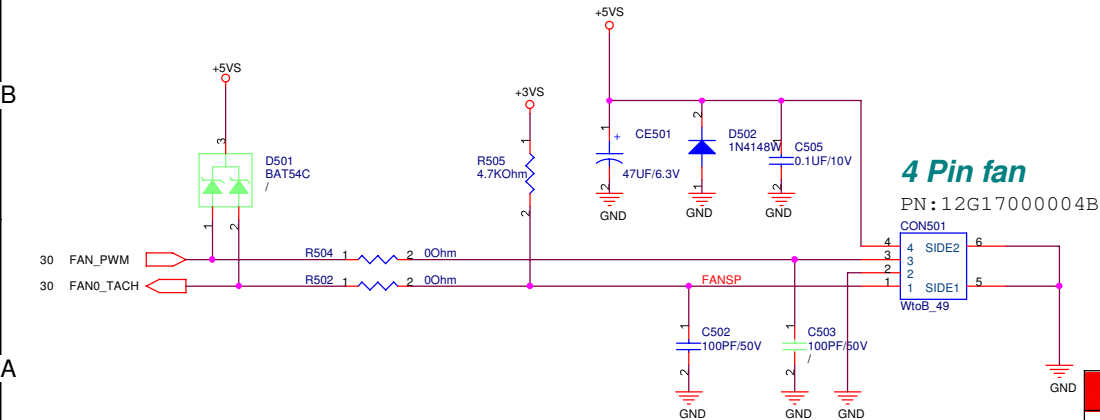
CLK MINICARD REQ# R432
4.7KOHM

		Title : Clock GEN	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size A3	Project Name F5V		
Date: 星期五, 四月 23, 2007		Sheet	4 of 94

Thermal Sensor



DC FAN Control



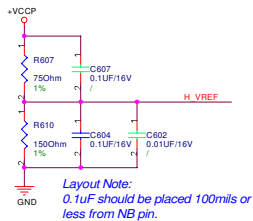
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
20 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
20 mils
-----OTHER SIGNALS

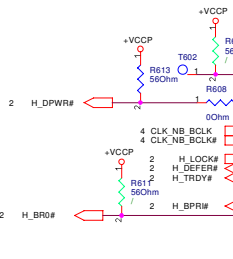
Avoid FSB,Power

ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size A4	Project Name F5V	Rev 1.0	
Date: 2007.04.23	Sheet 5 of 94		

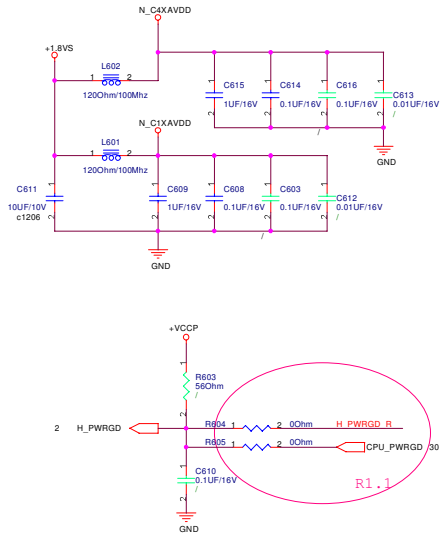
D



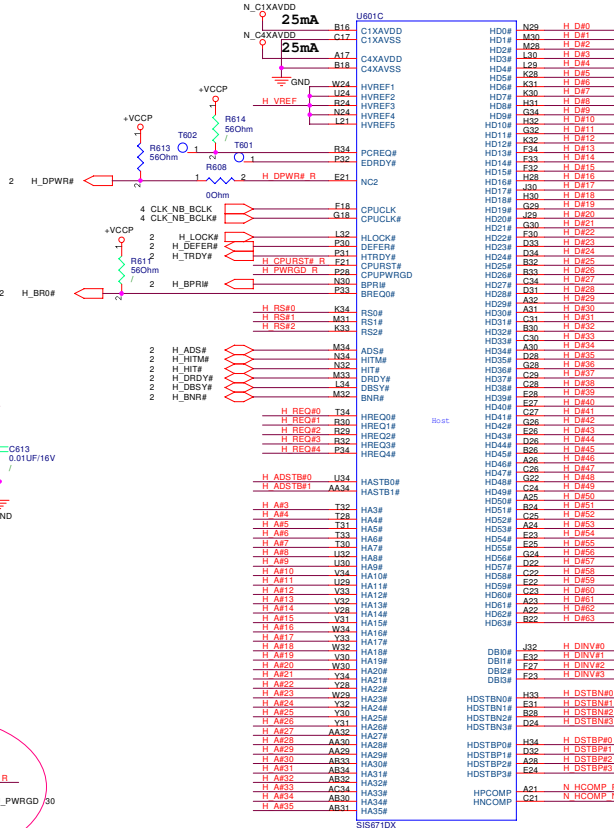
C



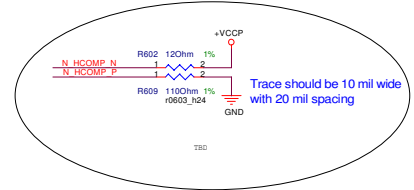
B



A



2



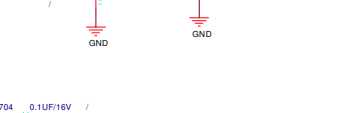
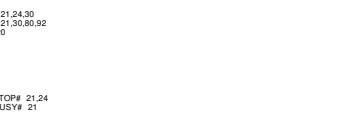
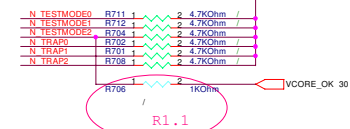
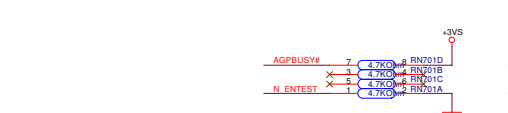
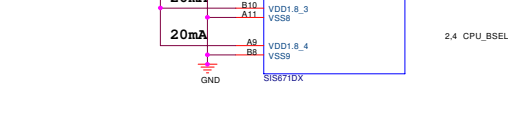
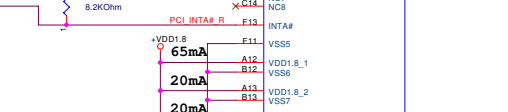
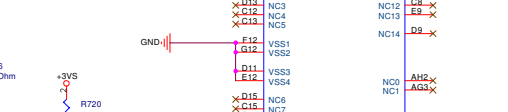
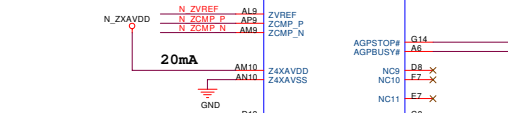
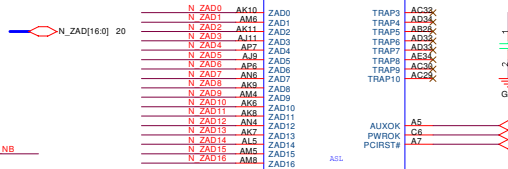
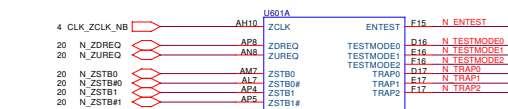
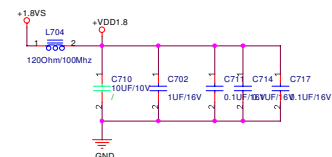
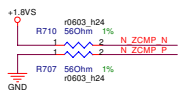
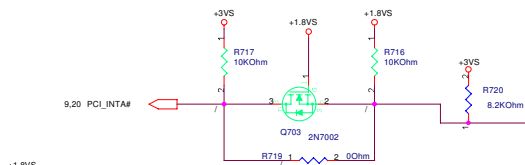
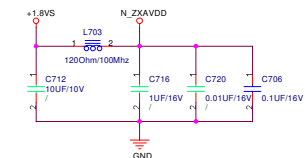
ASUS Title: M671DX (HOST)

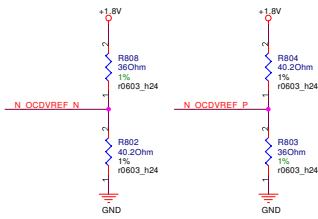
ASUSTek Computer INC Engineer: Hawk Zhu

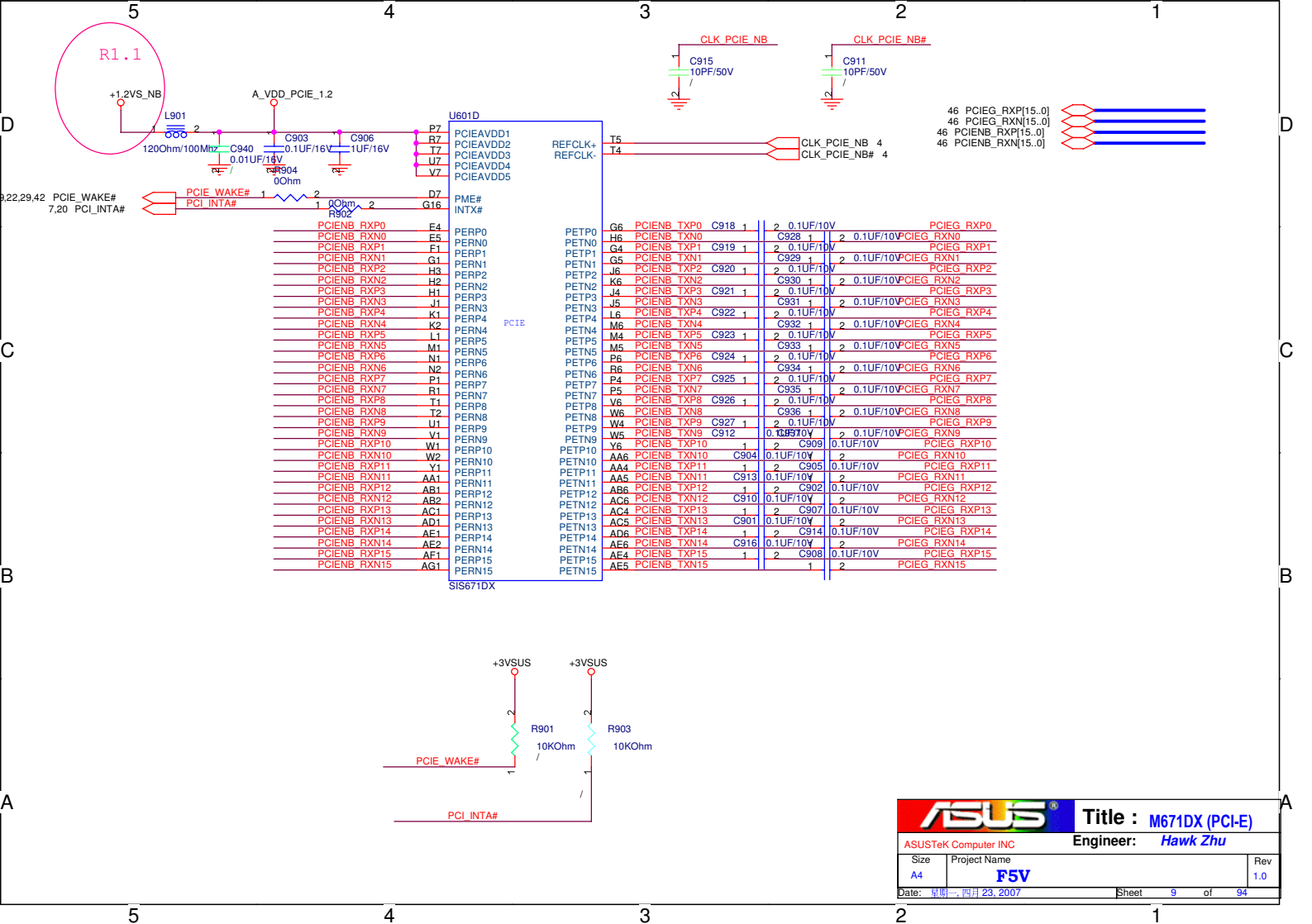
Size A3 Project Name F5V Rev 1.0

Date: 8/8/2007 Sheet 6 of 94

A



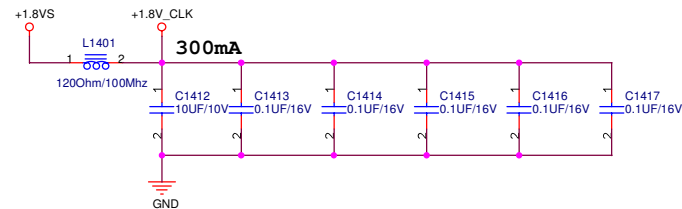
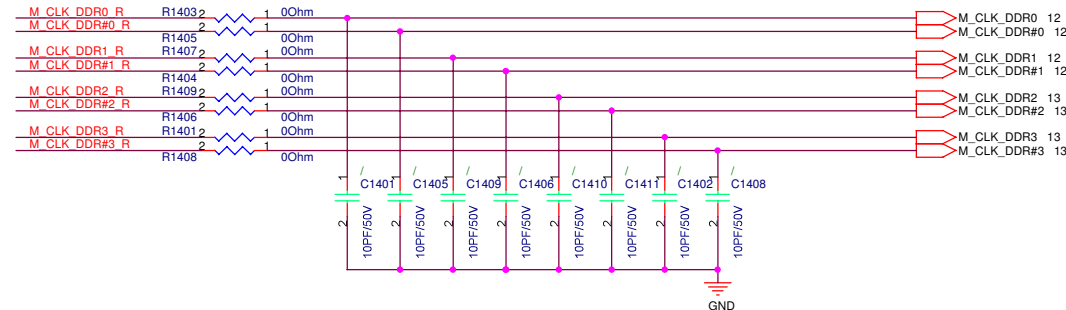
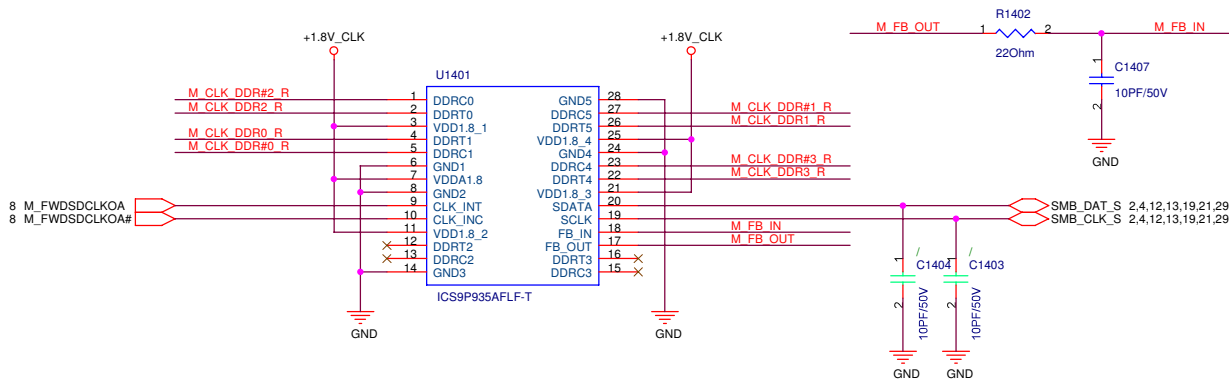


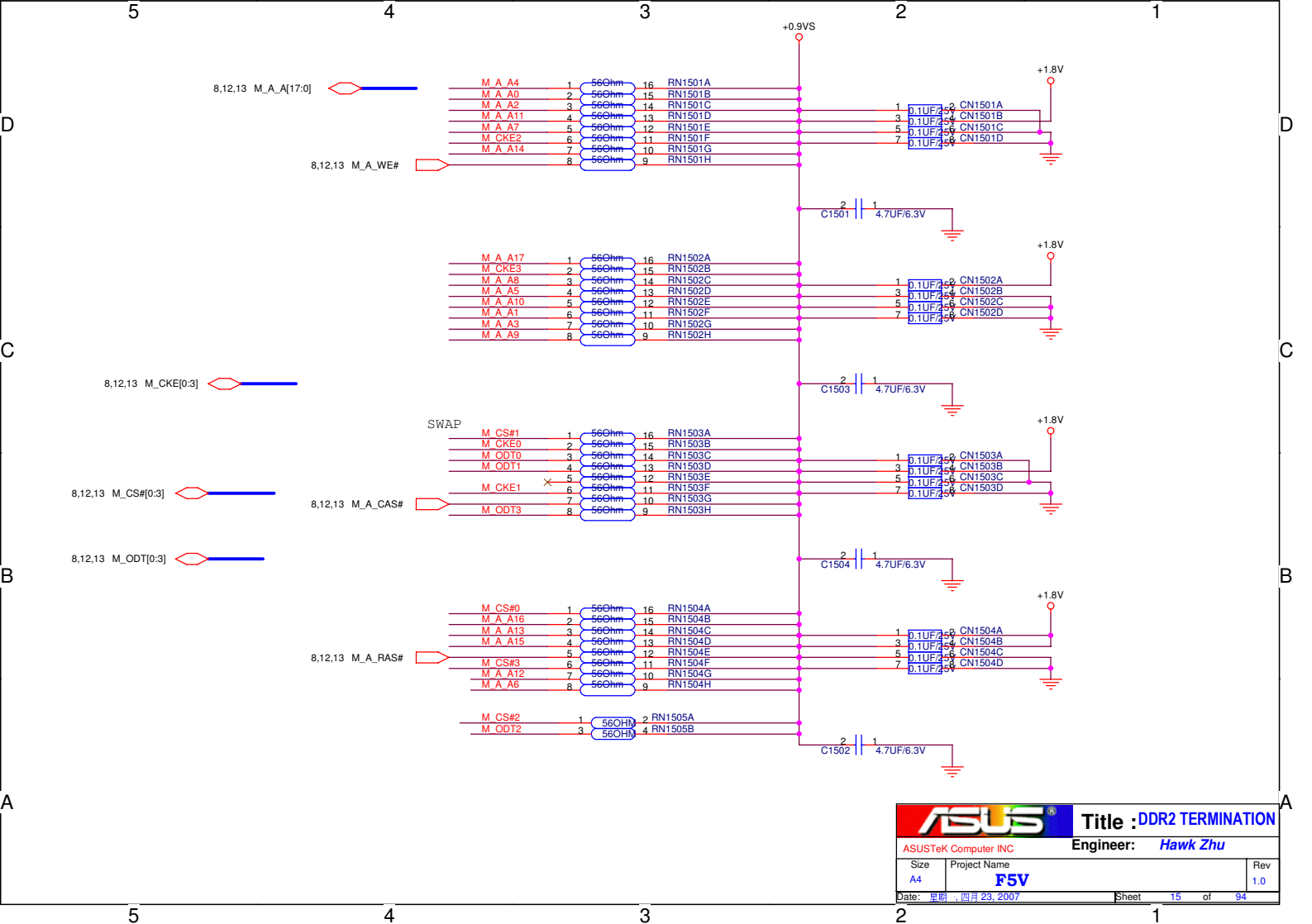




PN:12G025122006





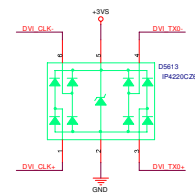
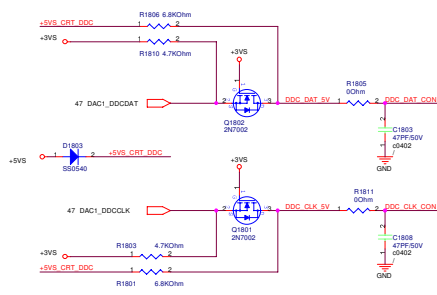
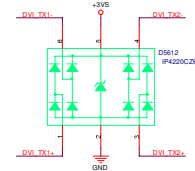
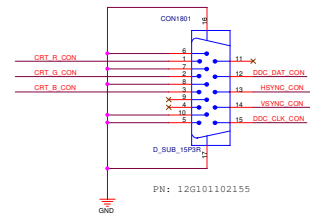


SI3865: US\$0.22

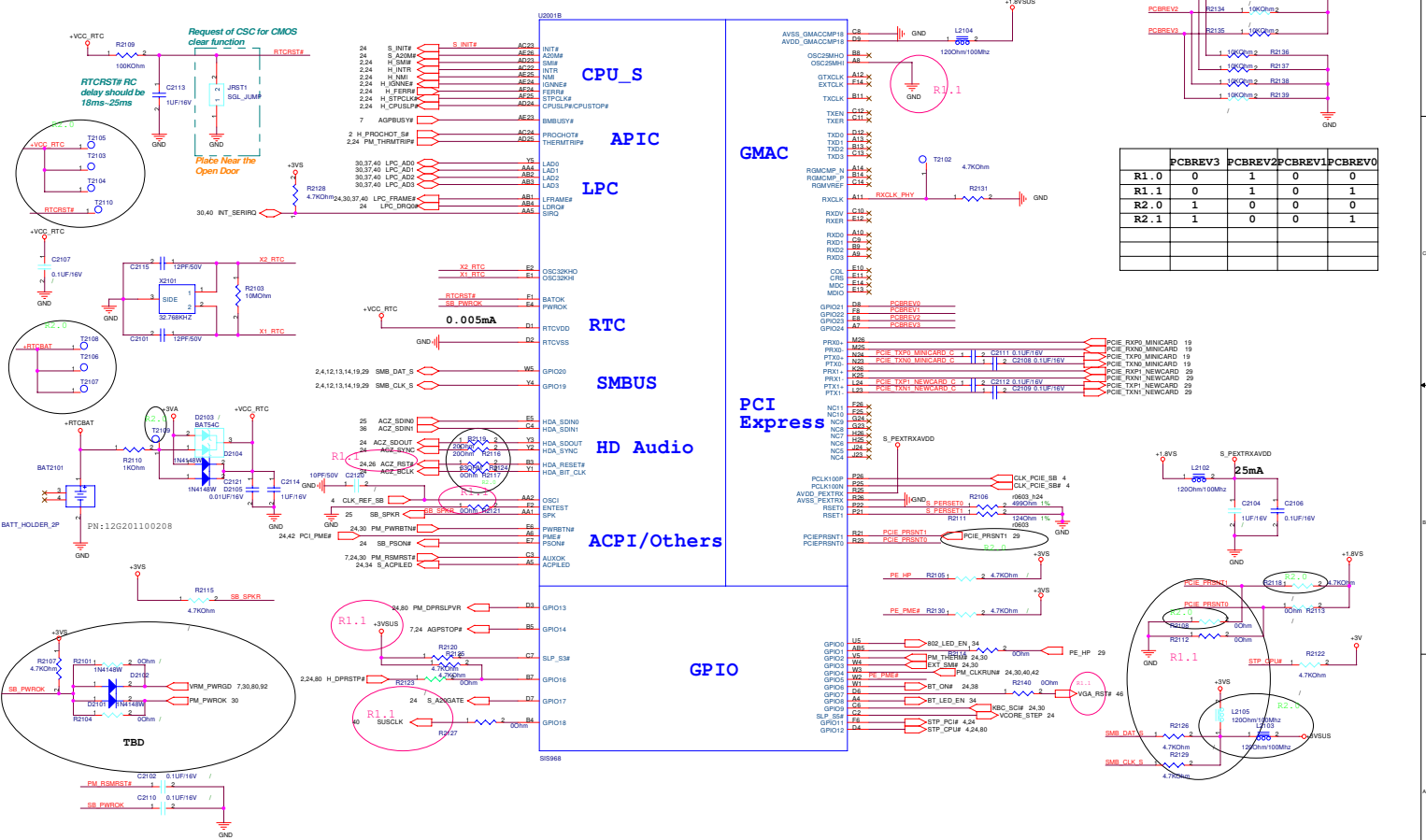


BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn
On/Off backlight
EC
INVER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

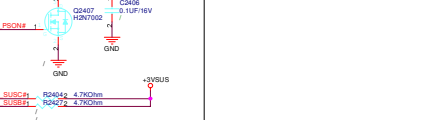
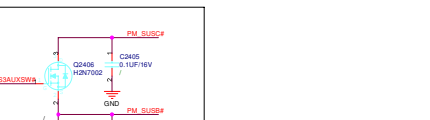
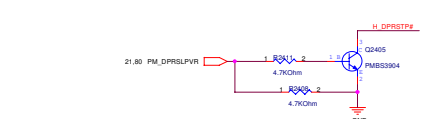
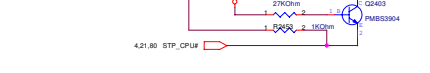
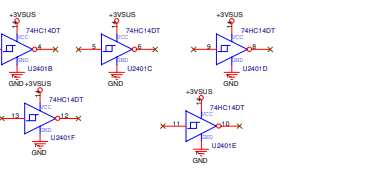
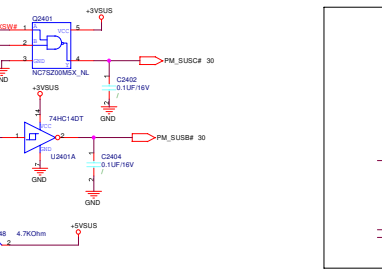
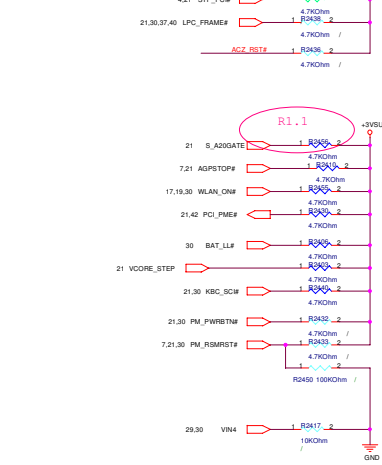
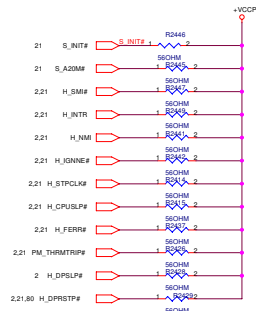
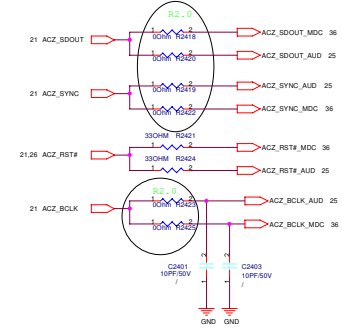
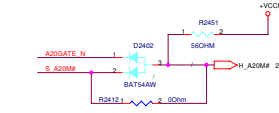
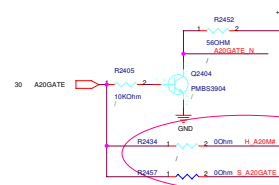
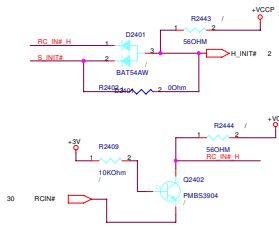


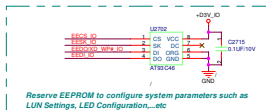
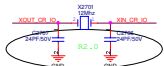
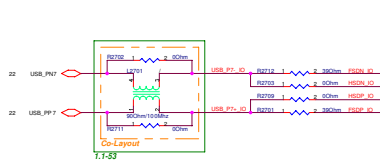




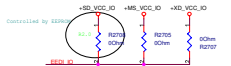


	PCBREV3	PCBREV2	PCBREV1	PCBREV0
R1.0	0	1	0	0
R1.1	0	1	0	1
R2.0	1	0	0	0
R2.1	1	0	0	1





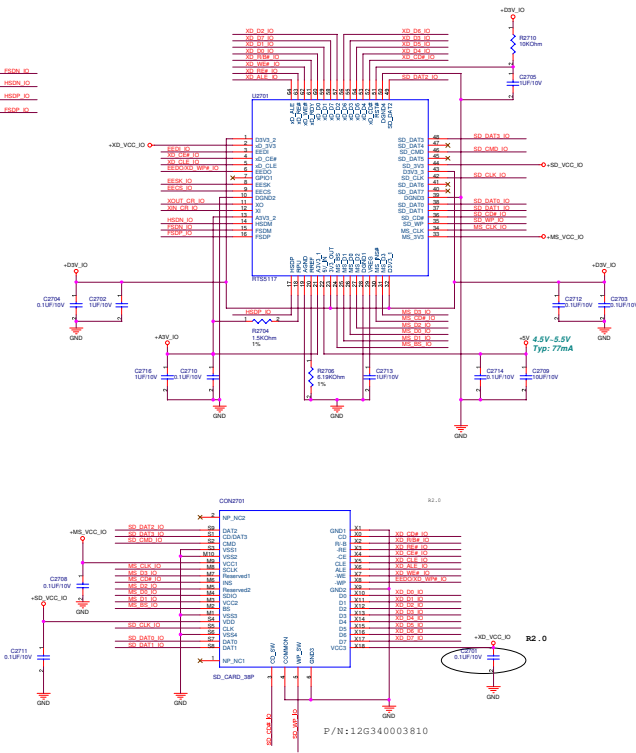
Reserve EEPROM to configure system parameters such as LUN Settings, LED Configuration...etc

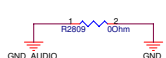
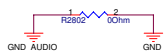
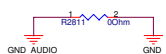
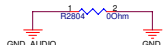
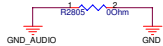


	IO_R2708 IO_R2705	
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC/MS/Pro Combo	No Stuff	4.7K
Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/Pro Combo	4.7K	No Stuff
Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/Pro Combo	4.7K	4.7K
Don't Support CPU C3 State	4.7K	4.7K

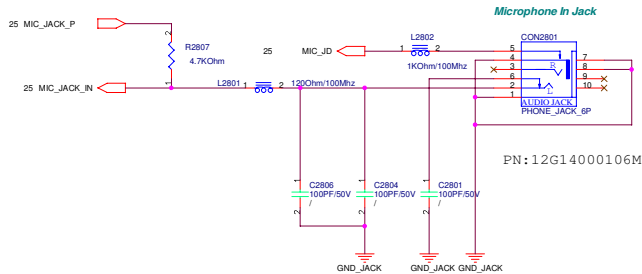
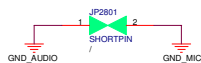
IO_R41 should be present if system doesn't use EEPROM to configure LED.

Through these pull-up resistors, EEPROM can be saved if no other requirement about other parameters.

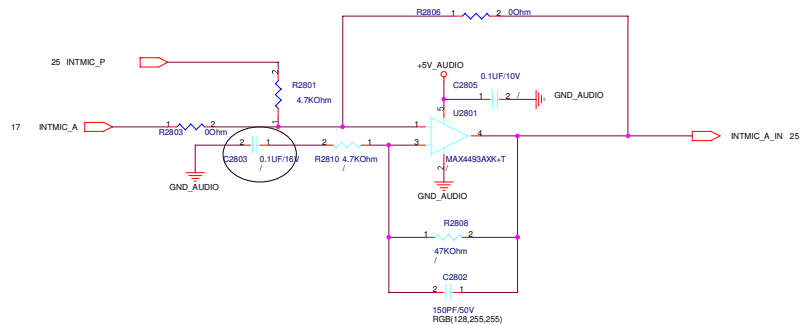




INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

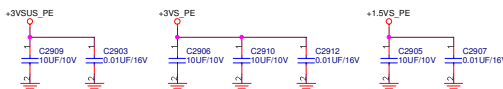
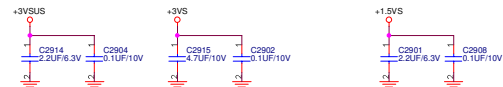
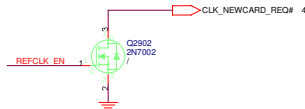
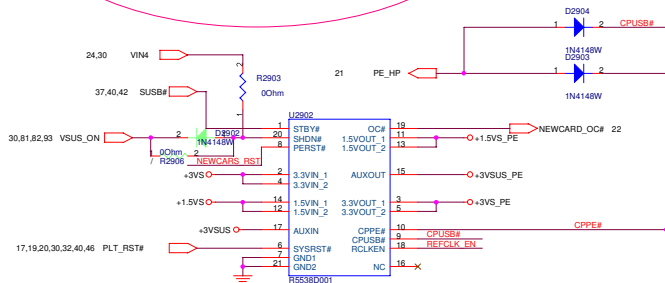
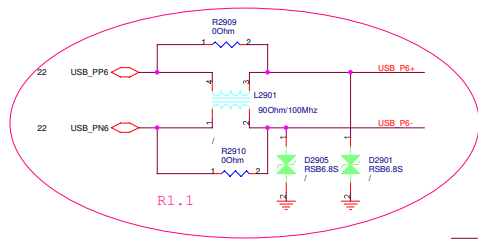


Pre-AMP For Test Function

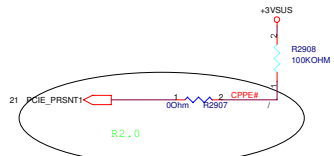
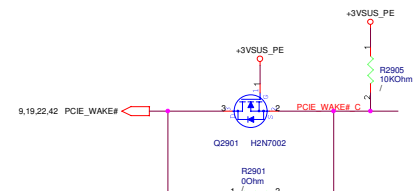
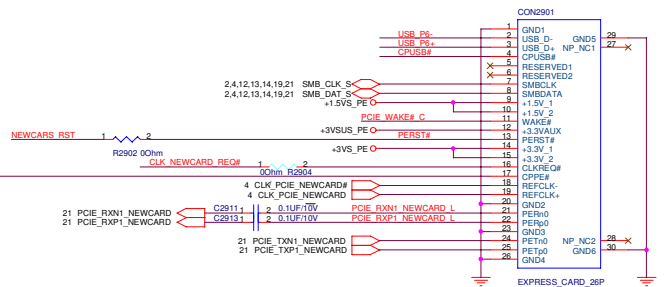


ASUS		Title : MIC,LINE-IN JACK	
<OrgName>		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	FSV		1.0
Date: 2017-11-24 20:07		Sheet 28 of 94	

FOR SWAP



!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



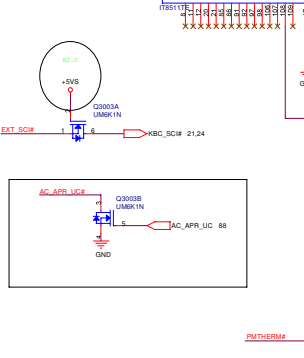
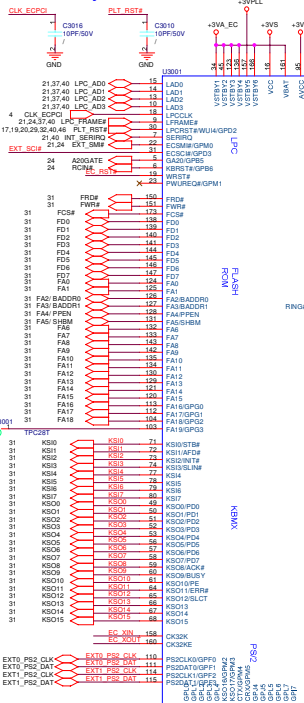
PN:12G161300261

PN:12G21C102604

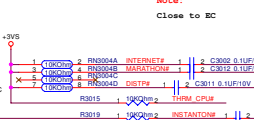
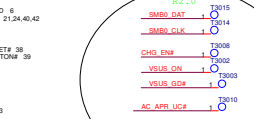
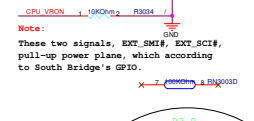
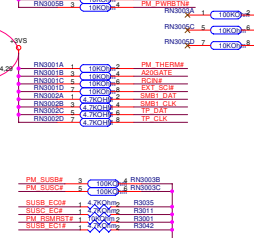
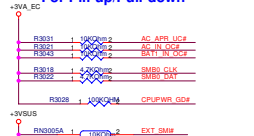
ASUS		Title : NEWCARD	
ASUSTek COMPUTER INC		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/11/2007	Sheet 29 of 34		

For IT8510 Core IC

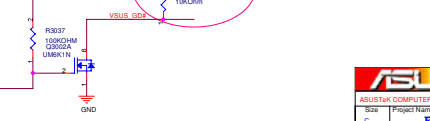
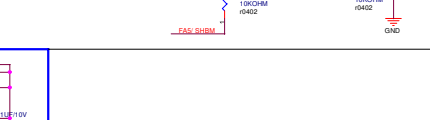
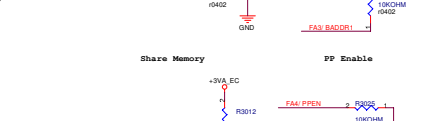
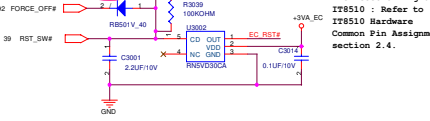
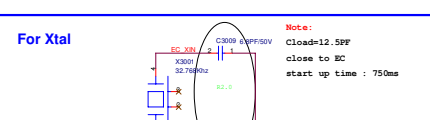
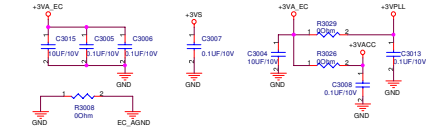
TQFP Package PN: 06G042003021
TQFP Package PN: 06G042003030



For Pill-up/Pull-down



For IT8510 Power



For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

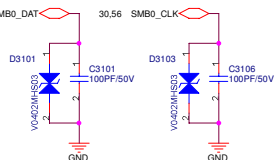
Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.

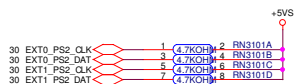
Note:

When we plug in or plug out the
battery, it may cause a spike to
damage the EC and gas gauge. It
needed to add these varistors to
protect those pins.

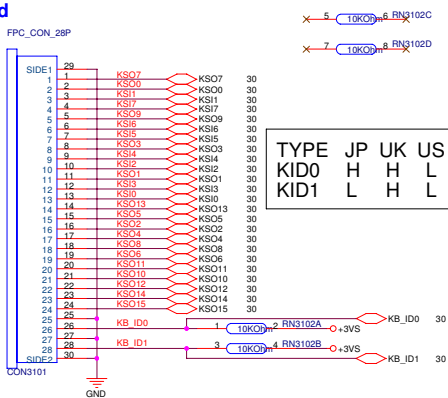
close to connector



For External PS/2 I/F

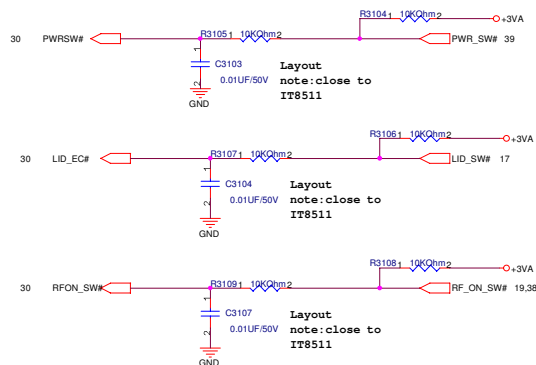


For Keyboard



TYPE JP UK US
KID0 H H L
KID1 L H L

For Switch



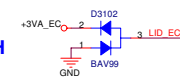
PWR SWITCH

LID SWITCH

RF SWITCH

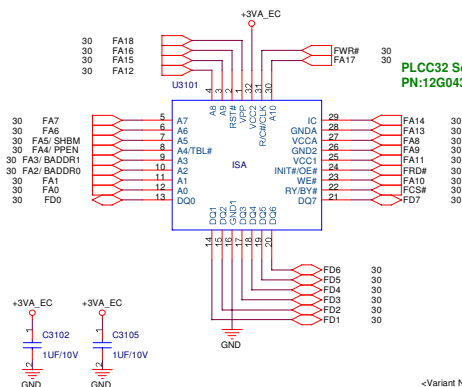
Note:

This LID_EC# is a signal
from inverter board, it is
easy to cause high voltage
damage when plugging
inverter board connector to
M/B with AC present. It
needed to add bidirectional
diode to protect this pin.



Layout
note: close to
connector

For 4M bits ISA ROM



Note:

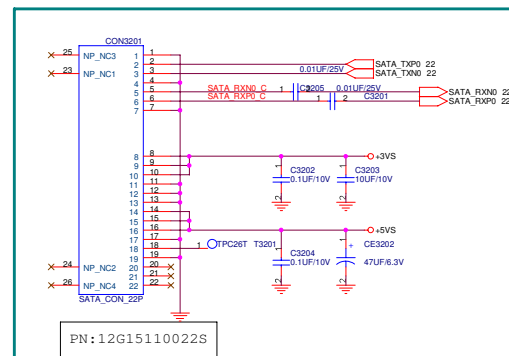
If you use 8M bits ROM, you need
to connect FA19 to EC side.

PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G00102721

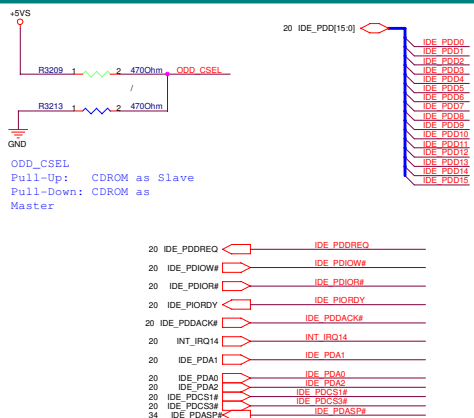
<Variant Name>

ASUS		Title :KB&ISA ROM	
ASUSTek COMPUTER INC. NBI		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 2007.01.23	Sheet 31 of 94		

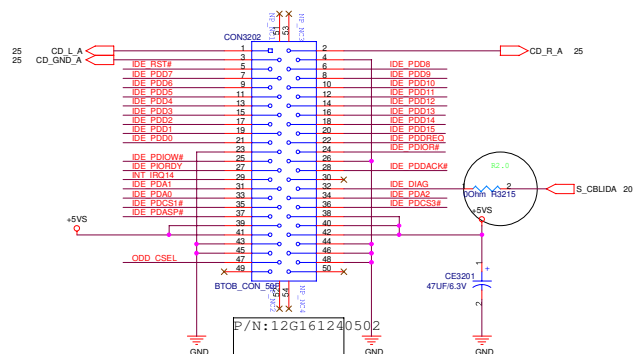


Dafult

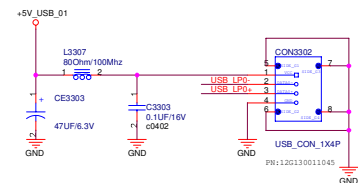
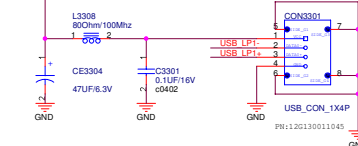
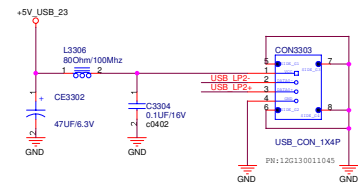
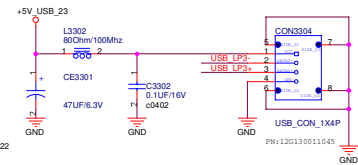
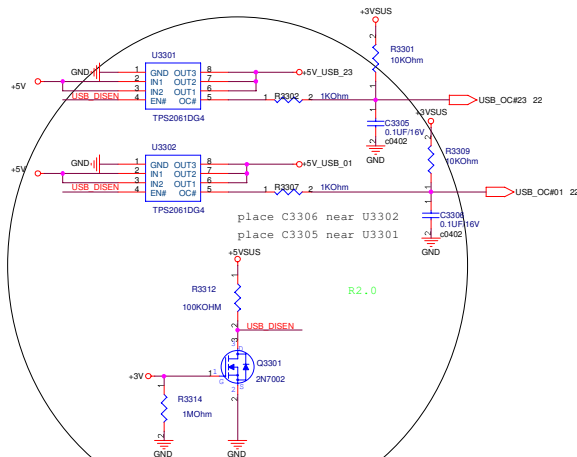
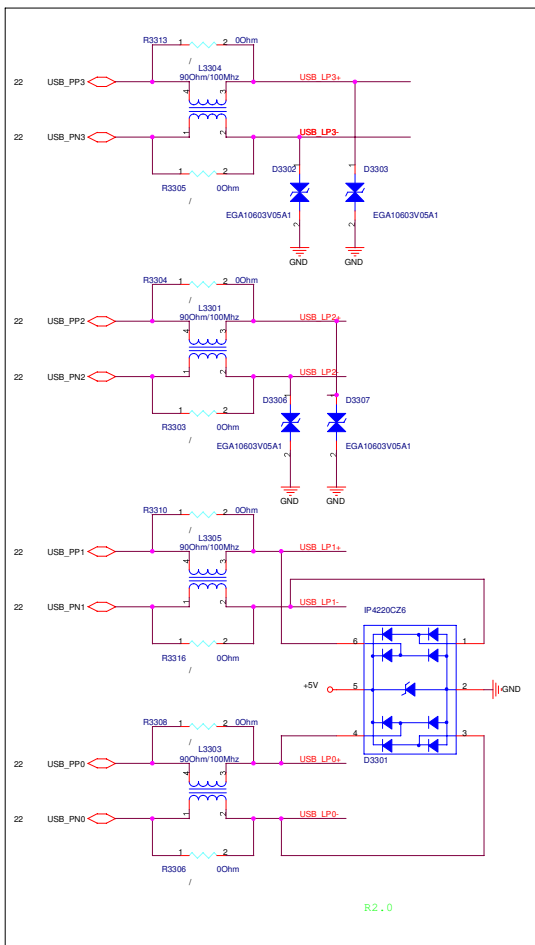
SATA



CD-ROM



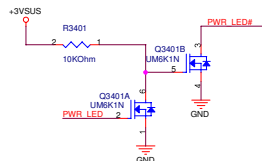
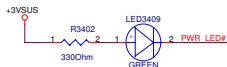
<Variant Names>



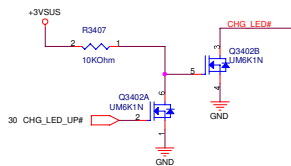
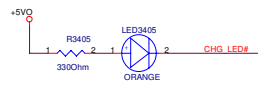
<Variant Name>

ASUS		Title : USB CONN	
ASUSTek COMPUTER INC. NBI		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 2007-10-23	Sheet	33	of 94

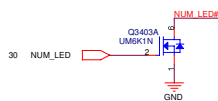
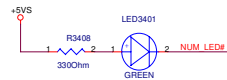
For POWER LED



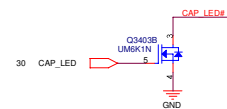
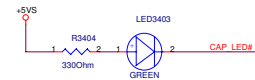
BATTERY LED



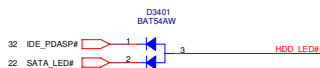
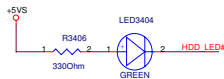
Num Lock



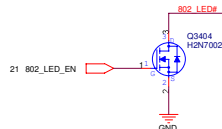
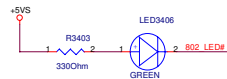
Cap Lock



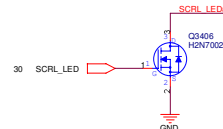
SATA/IDE LED



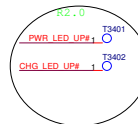
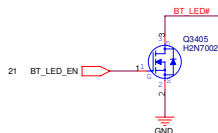
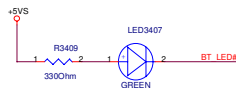
WireLess LED



Scroll Lock

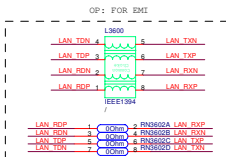


BT LED



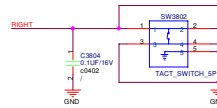
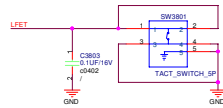
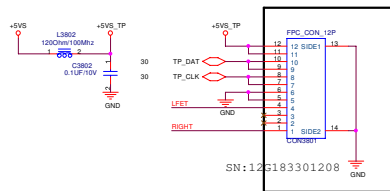
<Variant Name>

ASUS		Title : LED	
ASUSTeK COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: JUL 11 2007	Sheet	34	of 34

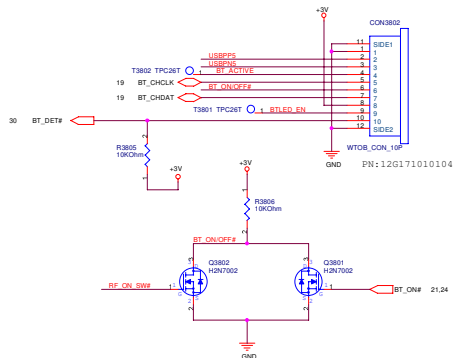
[illegible]

Touch-Pad

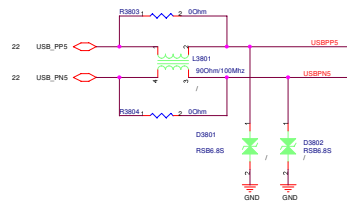
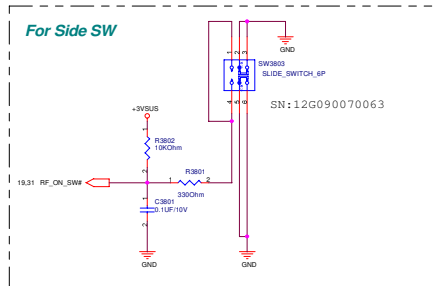
R1.1



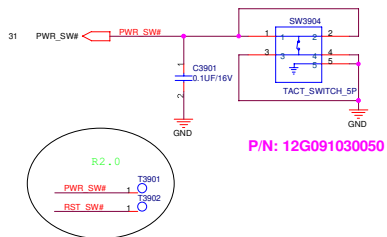
For Bluetooth



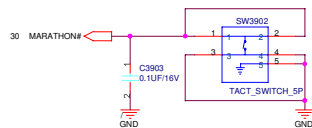
For Side SW



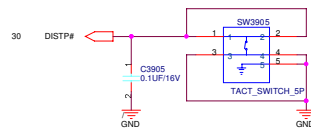
Power SW.



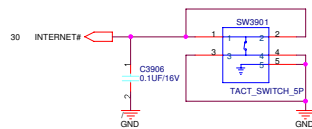
Marathon SW.



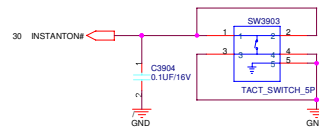
Disable Touch Pad SW.



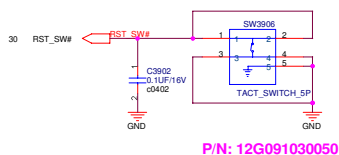
Internet SW.



IstantON SW.

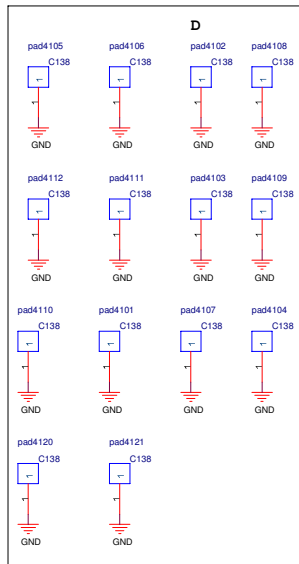


RESET SW.

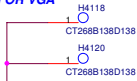


<Variant Name>

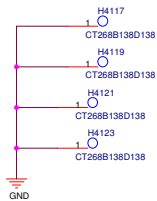
ASUS		Title : SWITCH	
ASUSTek COMPUTER INC		Engineer: Kaxidy jiang	
Size	Project Name		Rev
Custom	FSV		1.0
Date: JUL - 11 2007		Sheet 39 of 34	



FOR VGA



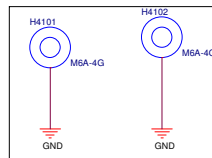
FOR CPU



FOR Mini card



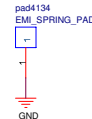
FOR MDC



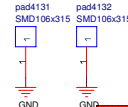
FOR FAN



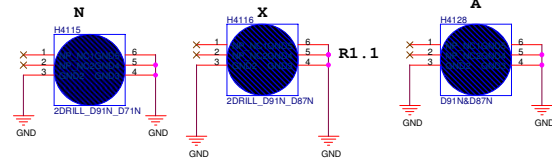
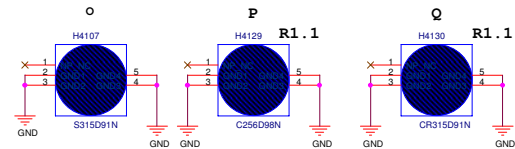
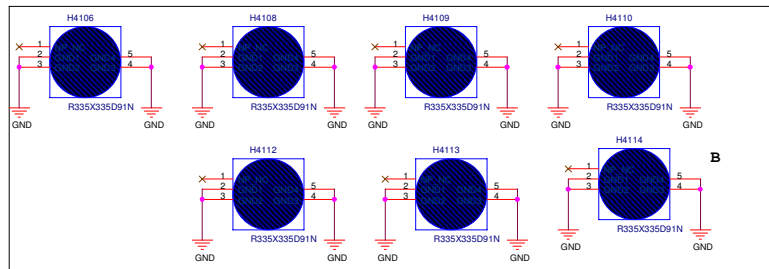
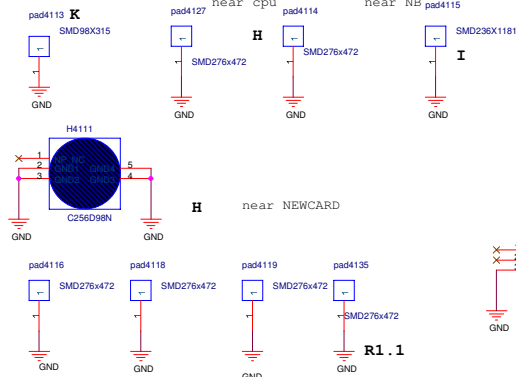
For EMI



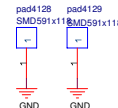
U



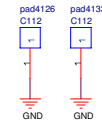
above ODD connector



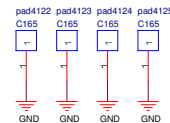
T



S

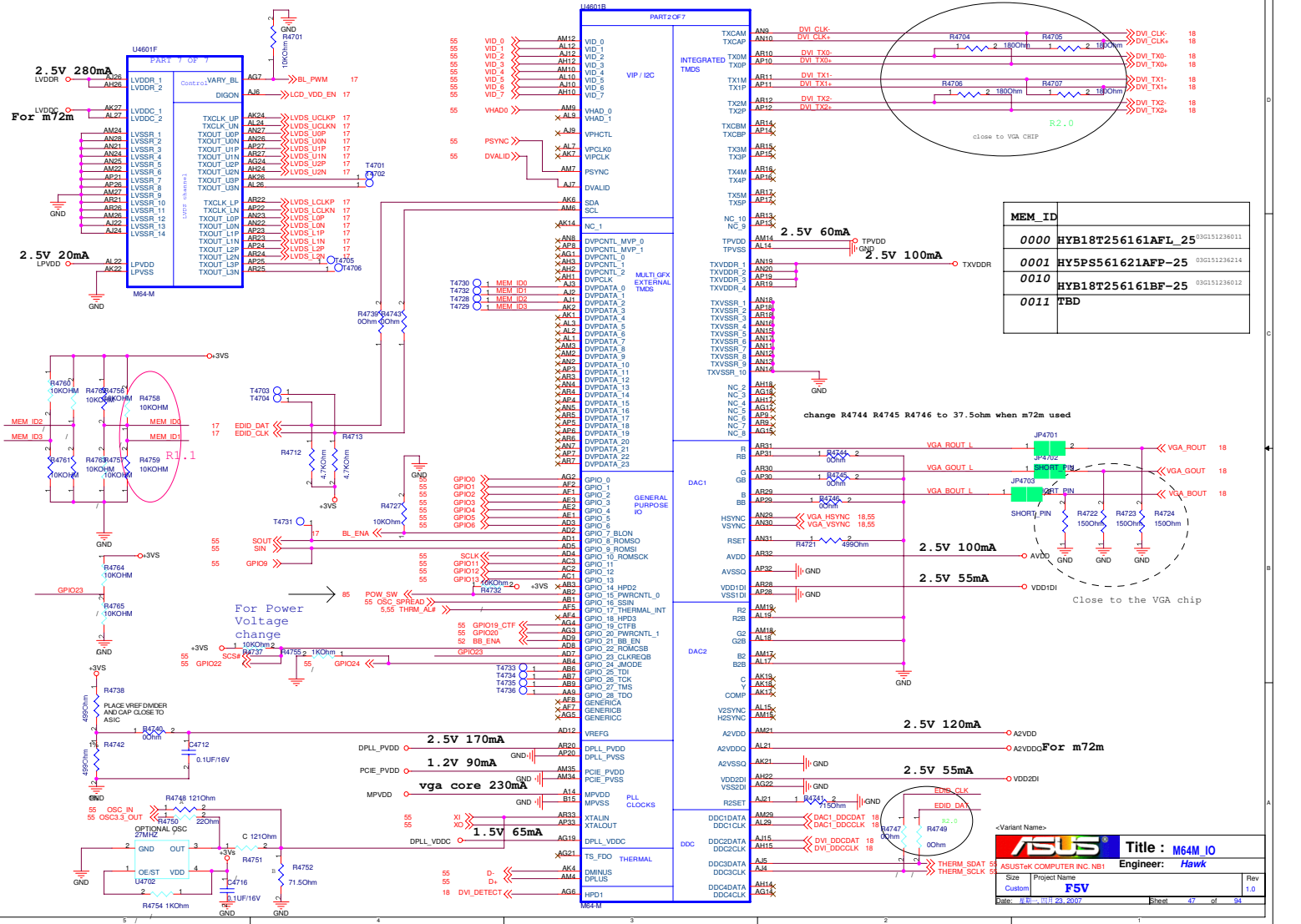


R



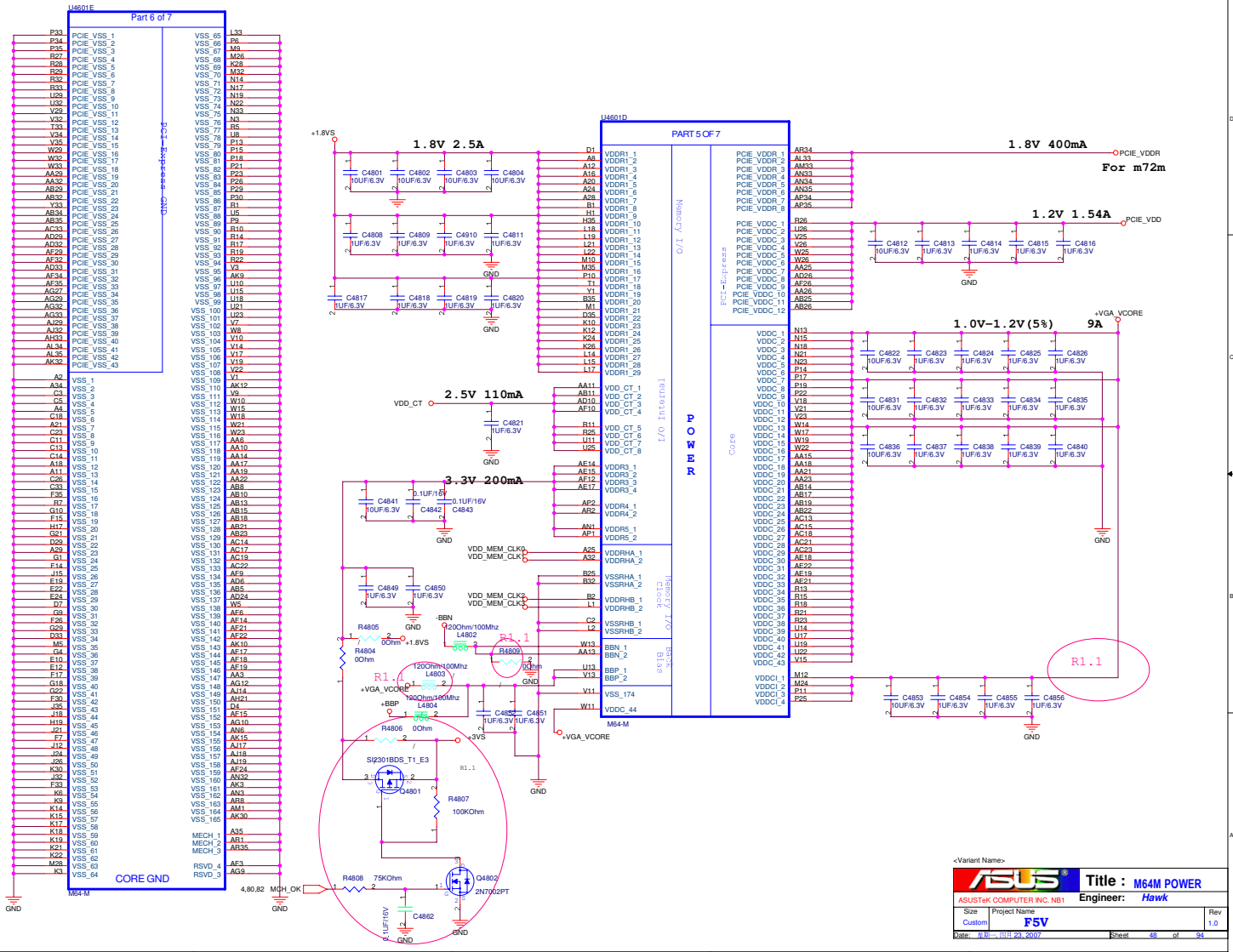
R2.0 change to P/N:13GN9980M090-1 for high limit

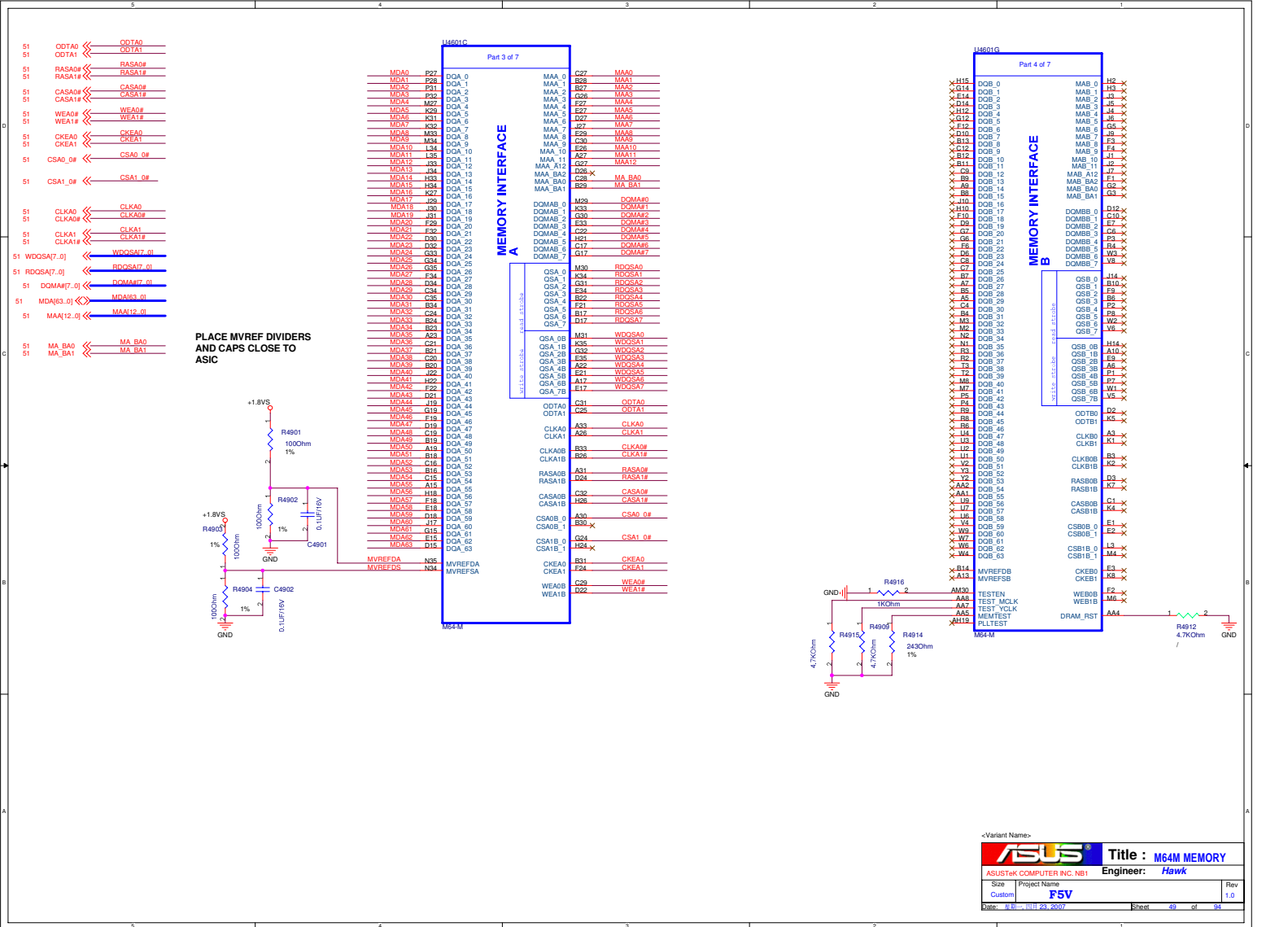
ASUS		Title : Screw hole	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name	Rev	
B	F5V	1.0	
Date: 11/01/23, 2007	Sheet	41	of 94

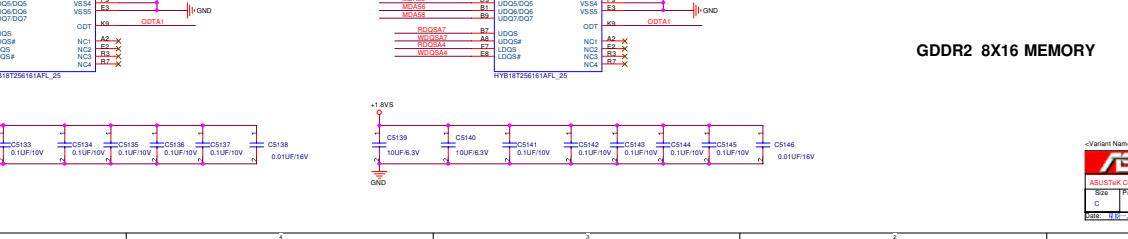
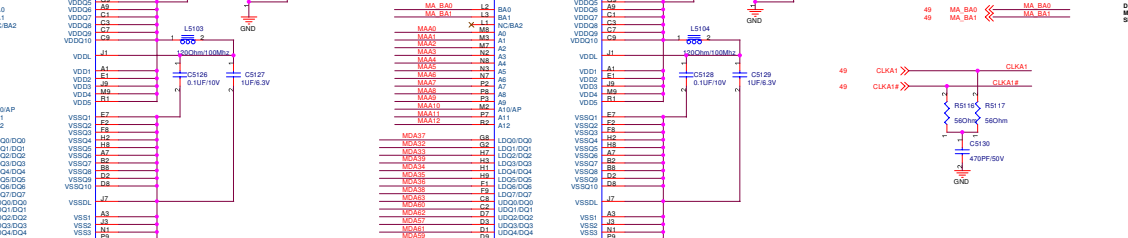
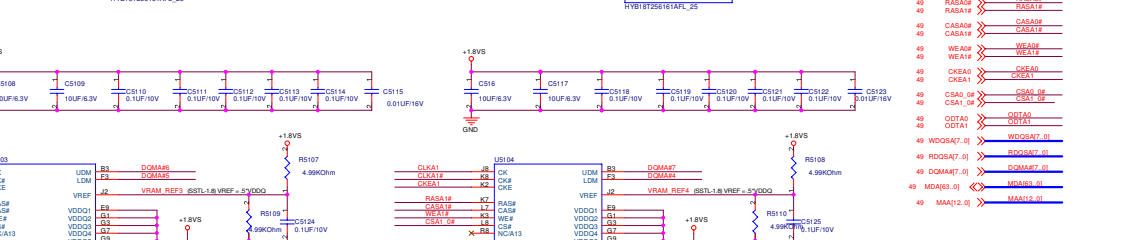
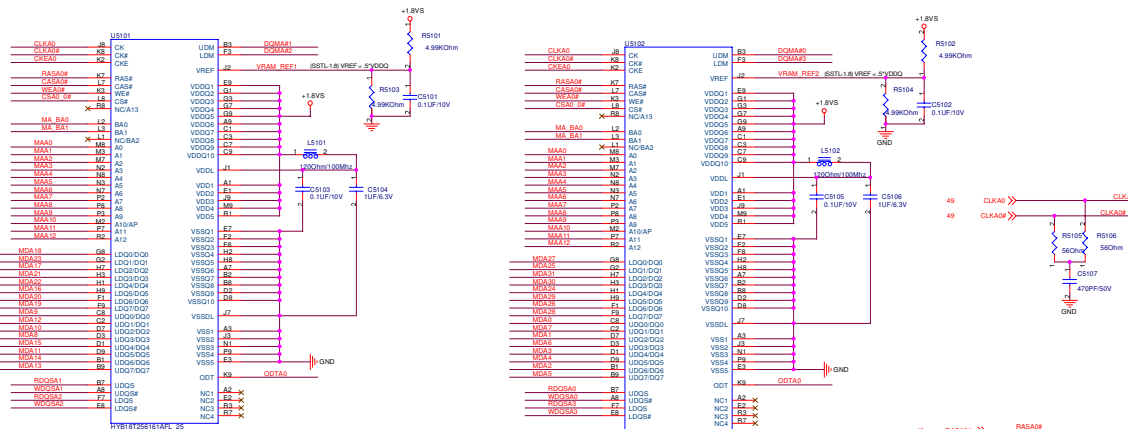


MEM ID		
0000	HYB18T256161AFL-25	03G151236011
0001	HYB5P561621AFP-25	03G151236214
0010	HYB18T256161BF-25	03G151236012
0011	TBD	

ASUS		Title : M4M IO
Size	Project Name	Engineer: Hawk
Custom	FSV	
Date: 11/01/2007	Sheet	47 of 94







GDDR2 8X16 MEMORY

**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

BB_ENA = 0V FOR BACK BIASING DISABLED

MAX1673 SHUTDOWN

-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND

N FET A = OFF, P FET B = OFF, N FET C = ON

+BBP = VDD_CORE

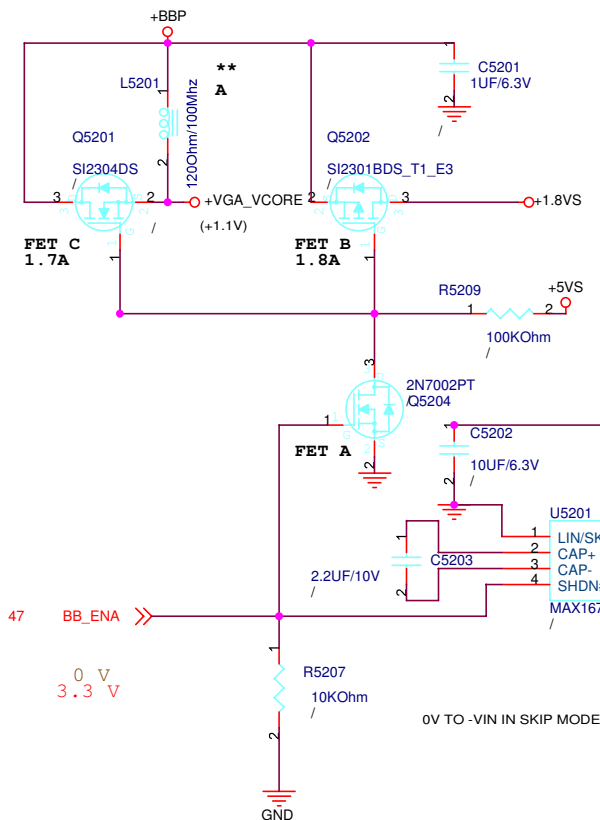
BB_ENA = +3.3V FOR BACK BIASING ENABLED

MAX1673 ENABLED

-BBN = -.5V

N FET A = ON, P FET B = ON, N FET C = OFF

+BBP = +1.5V



** FOR NO BACK BIASING

DO NOT INSTALL FETS OR REGULATOR LOGIC
AND INSTALL BEAD A AND RESISTOR A

(-.52V OR 0V @ 125MA MAX)



Title : **BACK BIAS**

ASUSTeK COMPUTER INC. NB1

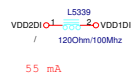
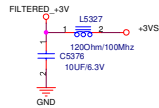
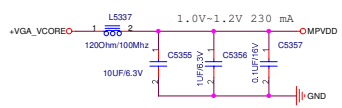
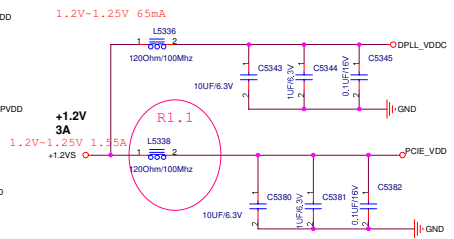
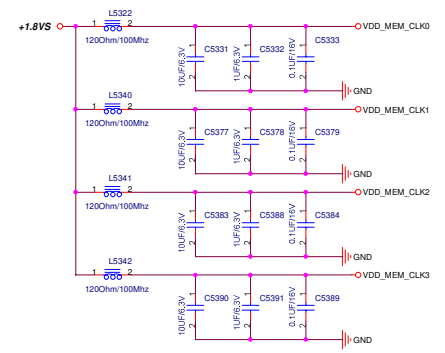
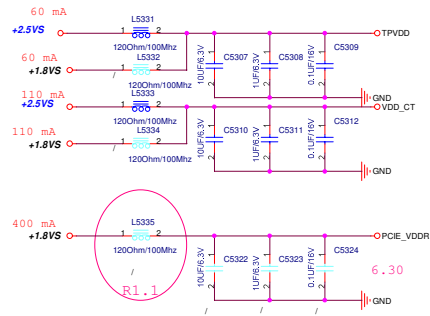
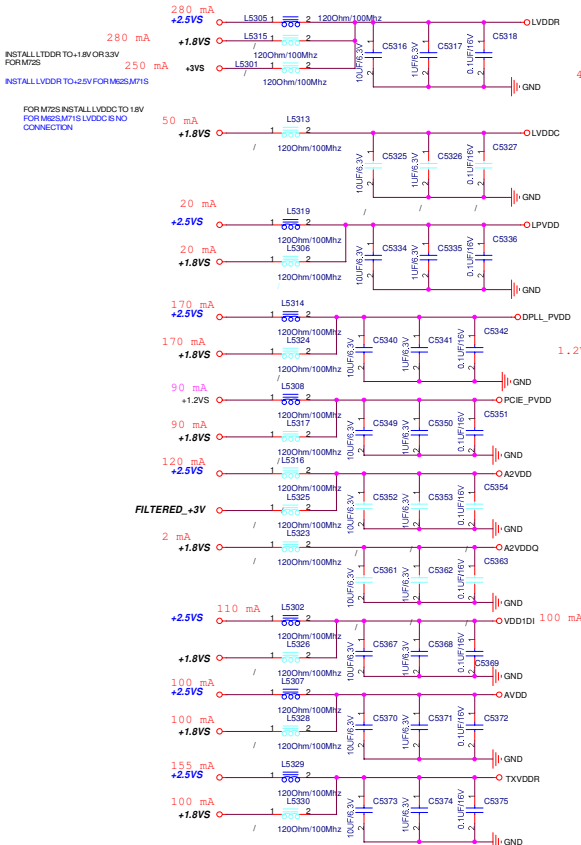
Engineer: **Hawk**

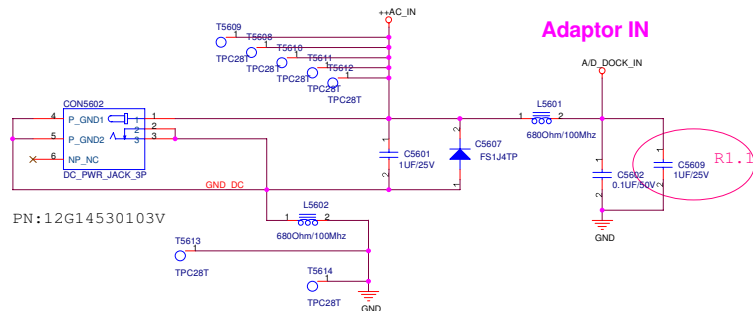
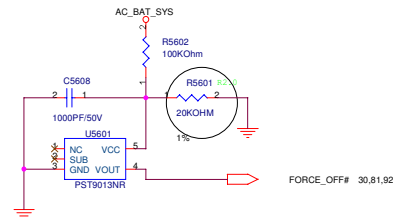
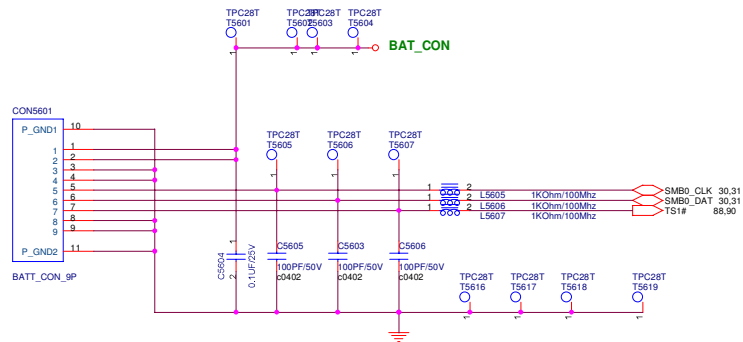
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007	Sheet 52 of 94	

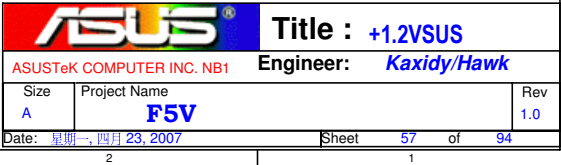
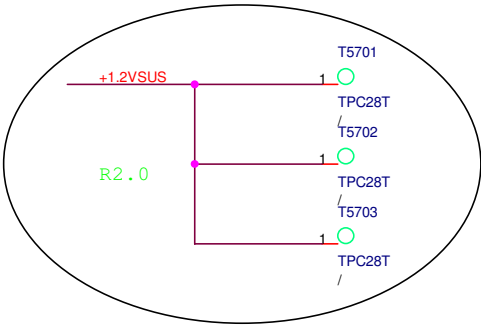
COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

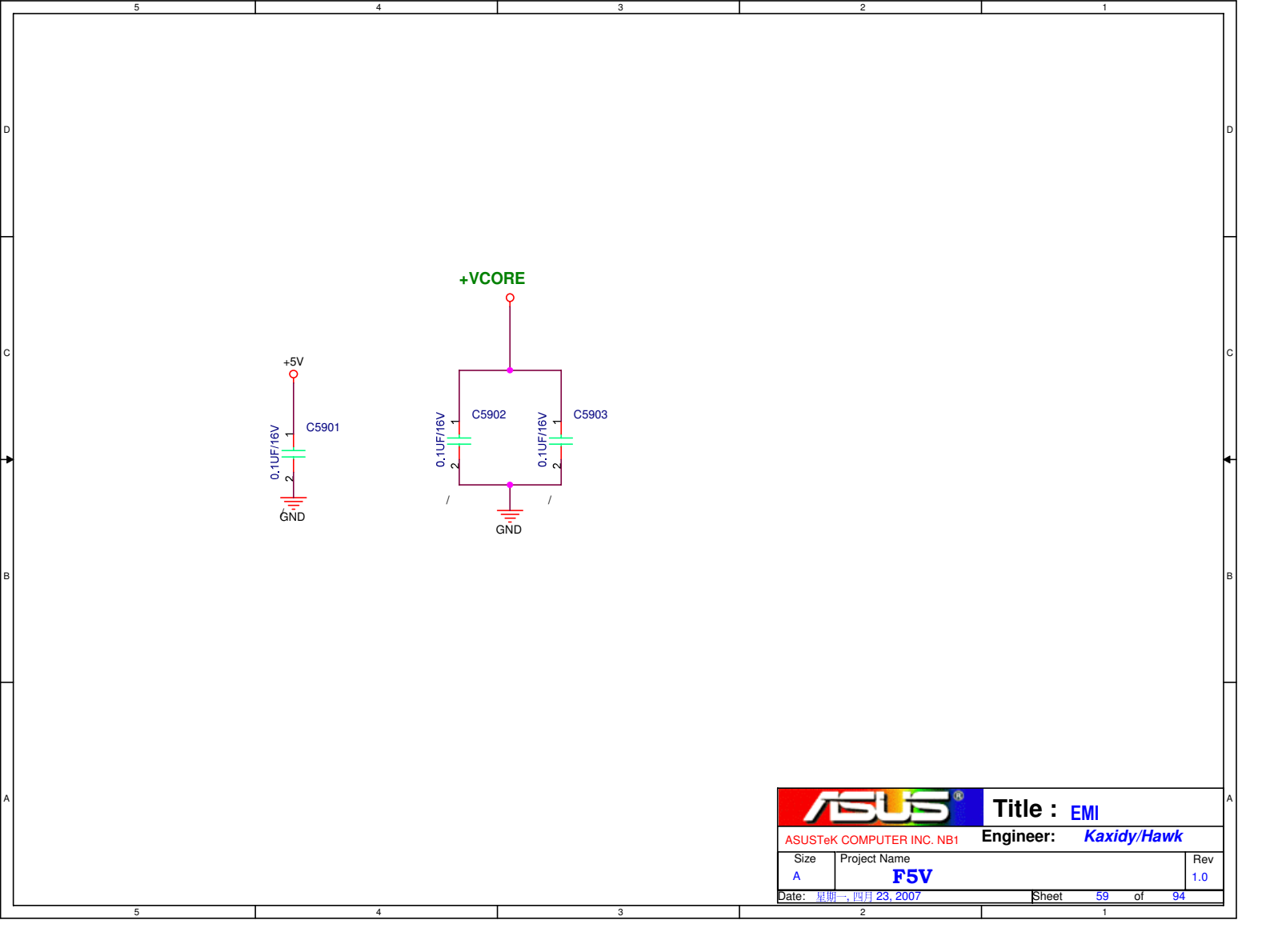
LTPVSS18 DVSSDI TPVSS MPVSS
* PCIE_PVSS PVSS A2VSSQ AVSSQ

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP









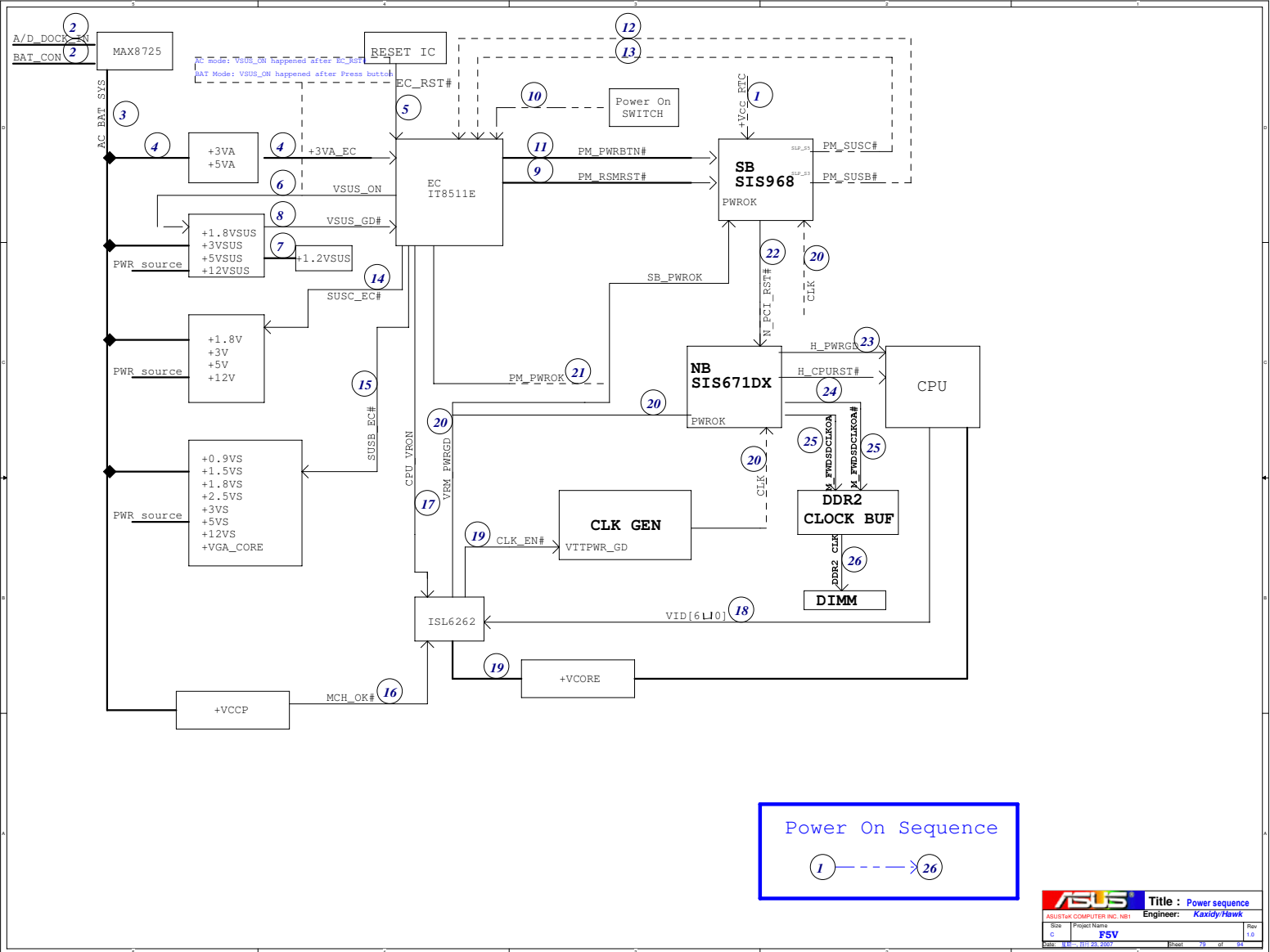
1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.
2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.
3. P7 unmount R706
4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]
5. P21 change R2121 to 00hm
add R2124(330hm) for AC2_RST# according to 968 ACT.
add R2108/R2112(00hm) for PCIEPRSNTO/1 according to sis ACT
add GMAC_OSC2SMII to QND according to sis ACT.
unmount L2103, mount L2105 according to spec.
unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
change GPIO17 from VIN4 to S_A20GATE, add R2127(00hm) for reserve SUSCLK
6. P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage
7. P22 change R2217 to 12K0hm, add C2237(22pF) for SATA REXT according to 968 ACT.
8. P24 add R2434 for A20GATE to H_A20M#, add R2457 for A20GATE to S_A20GATE, add R2456 to PU S_A20GATE
9. P29 add R2909/R2910(00hm), unmount L2901 for EMI.
10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .
delete D3004 for DDR power are not SUS power,
add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,
Add R3019 for INSTANTON#
11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost
12. P37 mount R3716/Q3715 for +VCCP discharge
13. P42 change IDSEL to PCI_AD24
14. P46 add D4602 for VGA_RST#
15. P48 unmount L4803/R4809, delete L4801
unmount R4806, mount Q4801/R4807/Q4802/R4808
16. P53 change L5335/L5338 to match the current.
17. P55 change X5501 to +-10ppm to follow spec, add C5508/C5509 to match X5501
18. P56 add C5609 for over current damaging charge IC.
19. P4 Change C440 from 0.1UF to 0.22UF
20. P10 change L1001 to 2A to match the current,, Add +1.2VS delay circuit.
21. P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.
22. P47 Unmount R4759, mount R4758 for Vram changed from 03G151236011 to 03G151236012.

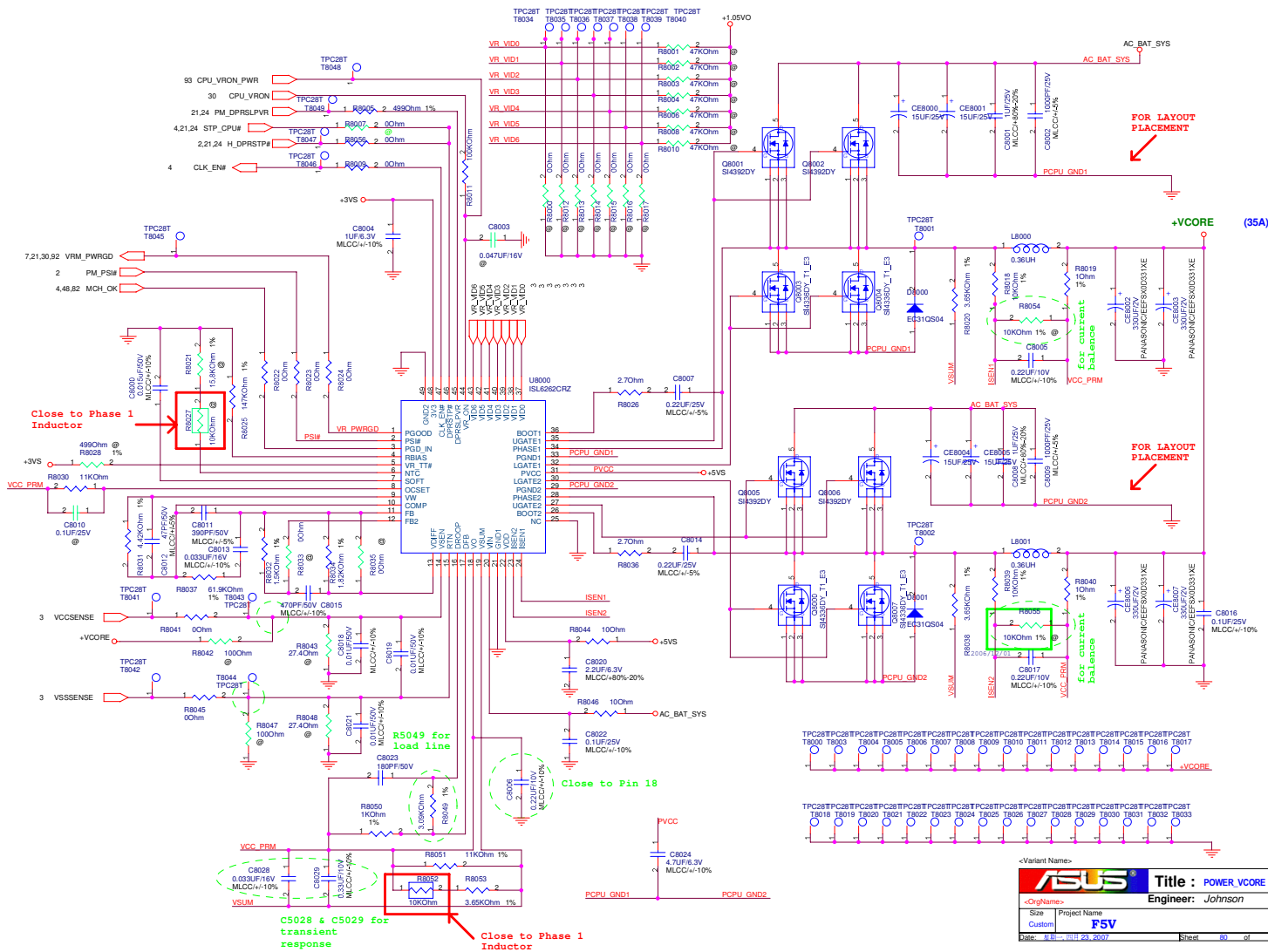
R2.0

1. P29 unmount R2907, connect PCIE_FRSNT1 to CFFE#
2. P21 unmount R2109, mount R2119, change R2118 from 00hm to 4.7K0hm but unmount R2118
2. P27 change R2708 to 00hm and mount it to not support C3 mode
3. P33622 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
4. P21 add R2141 to connect OS#_OC to PM_THRMTRIP#, change R2141 to Q2101
5. P30 change C3009/C3003 to 6.8pF
6. P27 change C2706/C2707 to 24pF
7. P55 change C5508/C5509 to 22pF
8. P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
9. P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
10. P30 change Q3003 PU from +5V to +5VS
11. P5 unmount R506
12. P56 change R5601 to 20K0hm
13. P20 unmount R2054, add and mount C2010
- P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
- P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
14. P27 change 4in1 cardreader
15. P47 mount R4704/R4705/R4706/R4707
- P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839, change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
16. P21 Unmount L2105, mount L2103
17. P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
P25 change R2514 from 330hm to 470hm

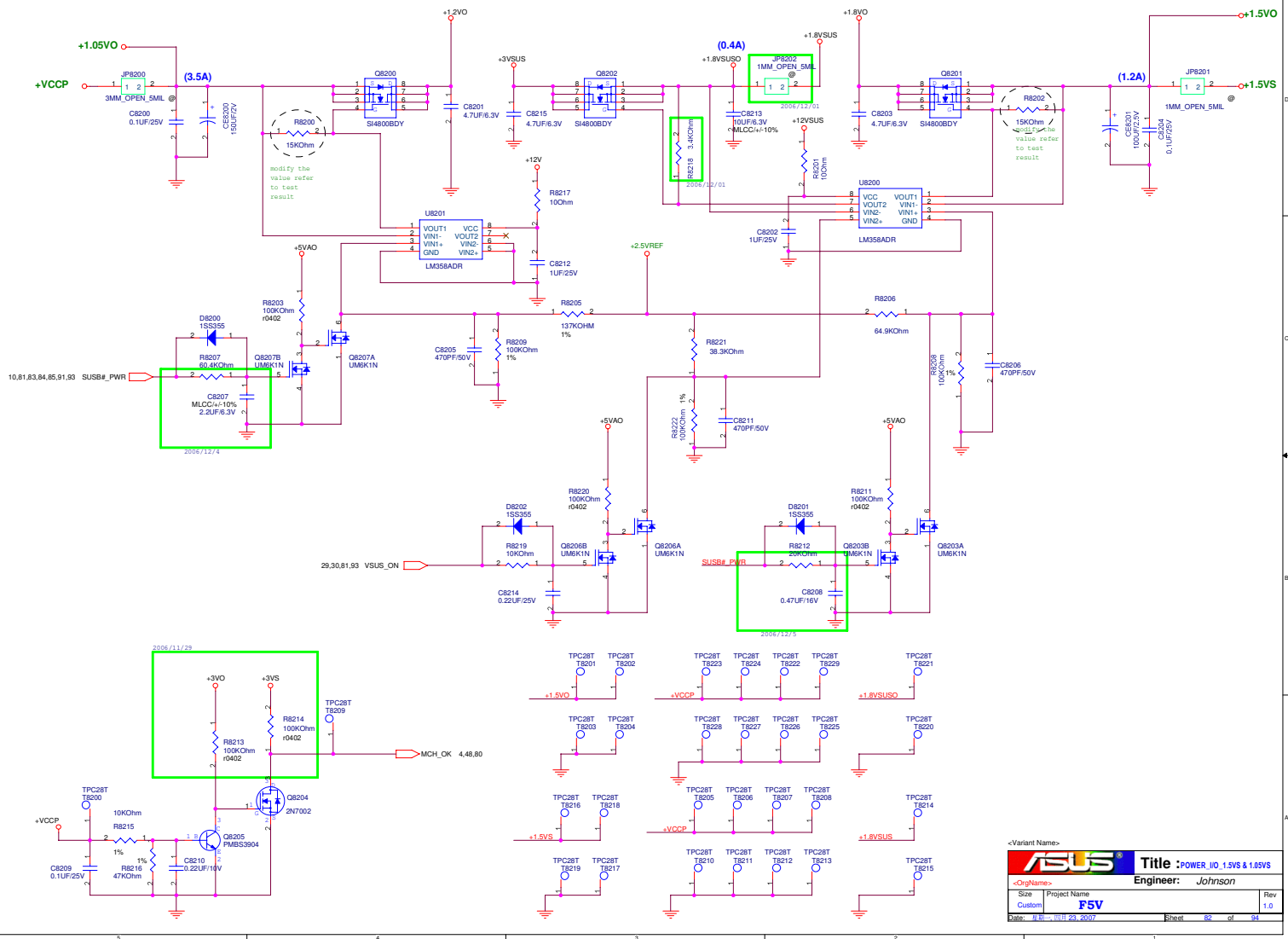
F5VL

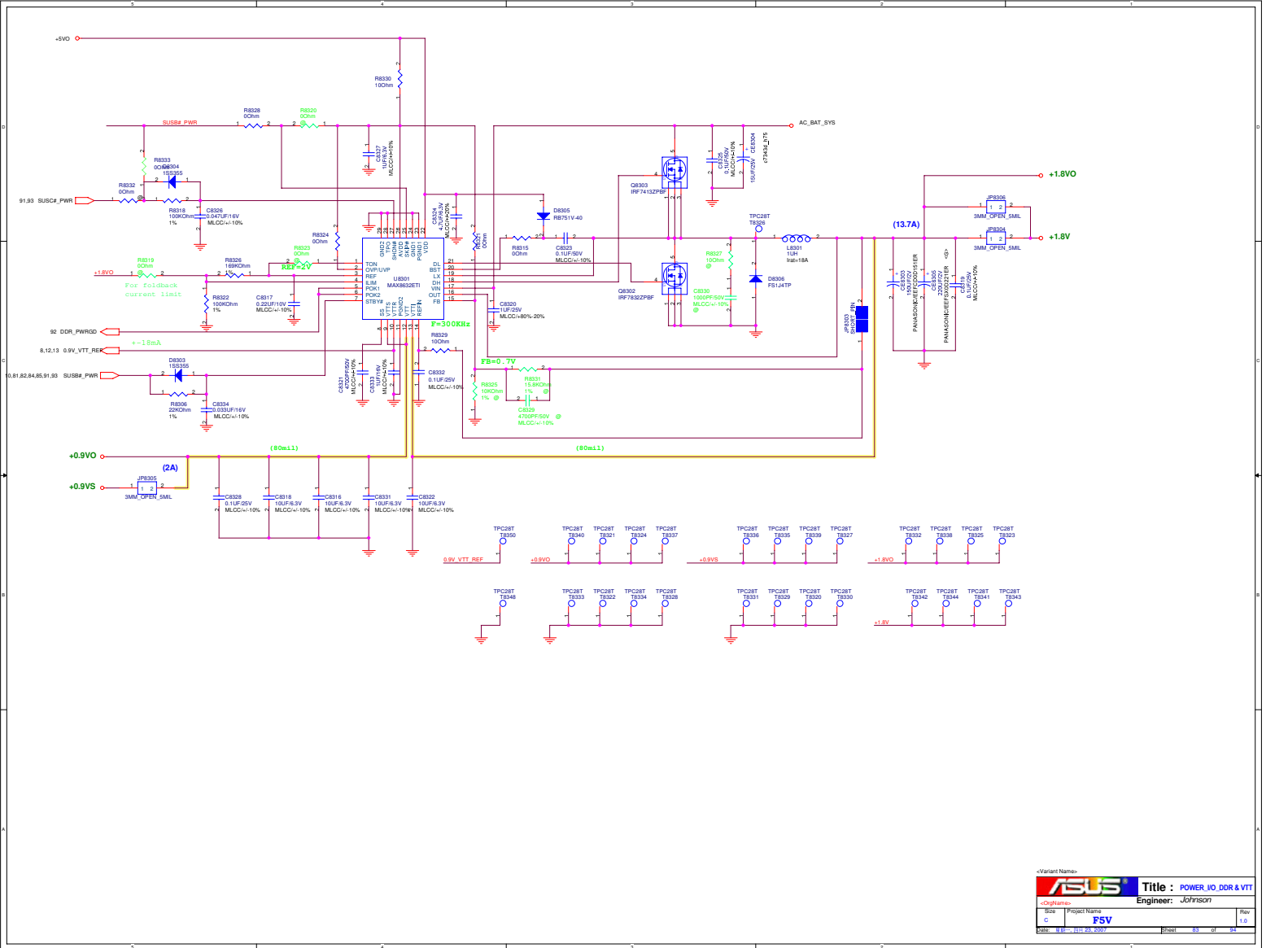
1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI



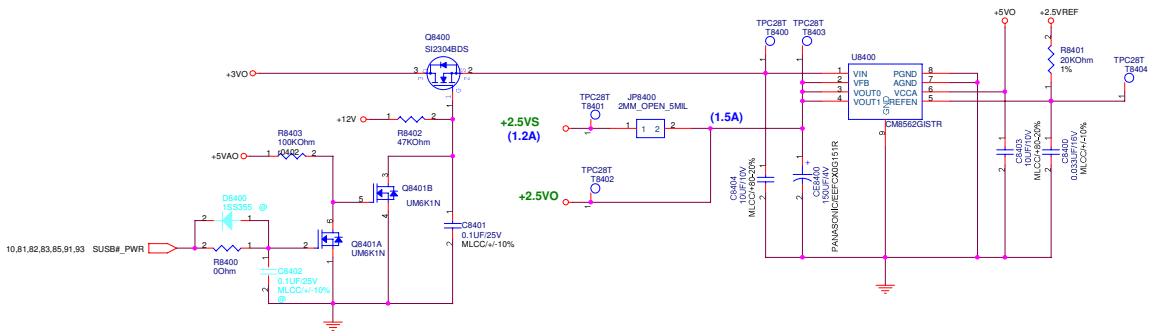


ASUS		Title : POWER VCORE	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: JUL 23, 2007	Sheet	80	of 94





+2.5VS



<Variant Name>



Title : POWER_I/O_+3VA & +2.5V

Engineer: *Johnson*

<OrgName>

Size	Project Name
Custom	F5

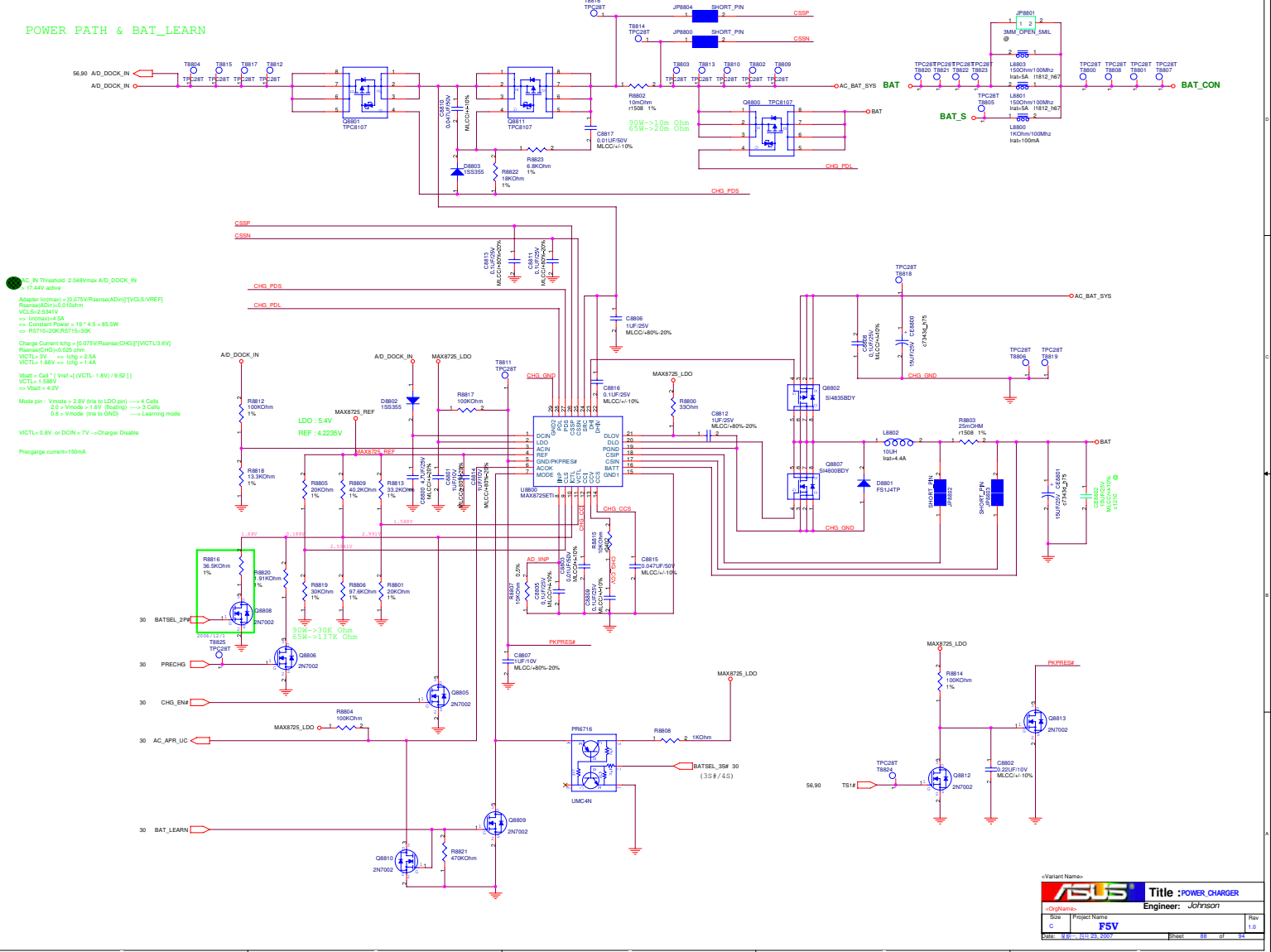
Rev

Size	Project Name
Custom	F5

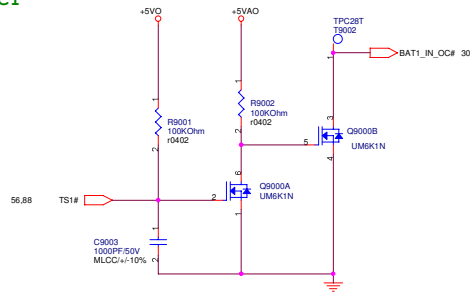
Date: 星期一, 四月 23, 2001

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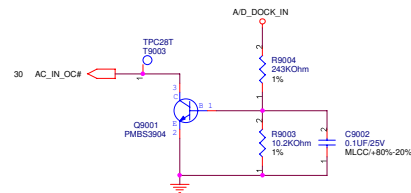
POWER PATH & BAT_LEARN



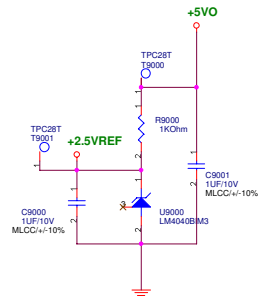
BATTERY IN DETECT



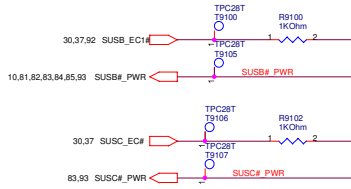
ADAPTER IN DETECT



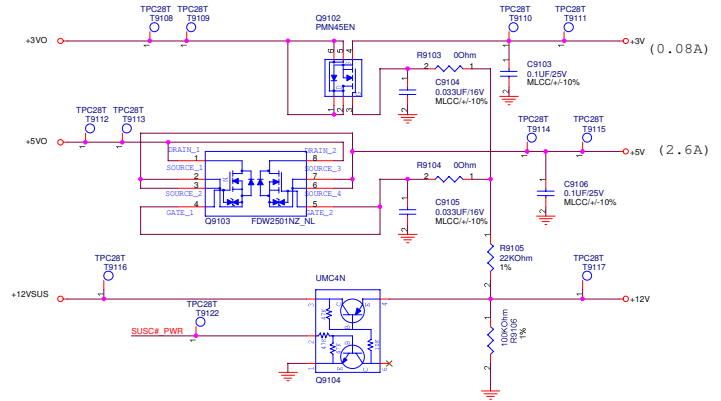
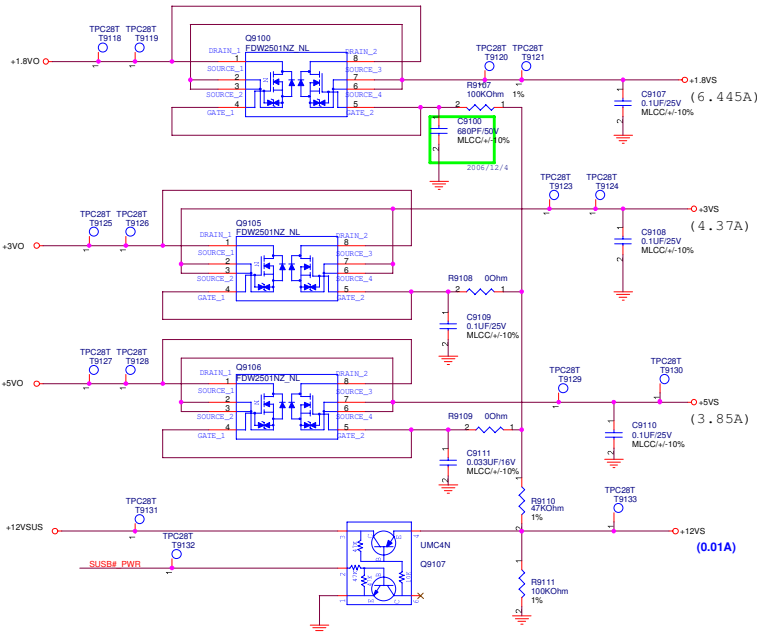
+2.5VREF



SUSC#_STAGE POWER



SUSB#_PWR POWER



ASUS		Title :POWER_LOAD SWITCH	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 10/11/2017	23, 2017	Sheet	91 of 94

POWER GOOD DETECTOR

